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Ph.D. THESIS SUMMARY

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SENZORI DE TEMPERATURĂ MONOLITICI AVANSAȚI

ADVANCED MONOLITHIC TEMPERATURE SENSORS

THESIS COMMITTEE

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Chapter 1
What is temperature? Why do we need to measure it?

The puzzle of measuring temperature has been largely solved. Precision thermometry may be achieved through a large range of methods (black body radiation [8], electrical potential or resistance, nuclear magnetic resonance [9], to name but a few). The outstanding problem is how to do so with as little costs, as conveniently and as precisely possible.

1.2 A never-ending trade-off: performance vs. cost

Accurate commercial thermometers are calibrated periodically at multiple points and / or characterised in tables with temperature intervals between points as low as $1°F$ [18]. These are generally very expensive devices and periodic calibration is a significant portion of total operating cost.

Industrial, automotive, medical, and meteorological thermometers are generally based on resistance temperature detectors (RTDs), thermocouples, thermistors or diodes with additional conditioning electronic circuitry [19] [20] [21]. These solutions cannot be integrated, and this fact sets a lower limit for their price.

At the lower end of the performance range we find cheap monolithic (in many situations disposable [22]) sensors, usually intended for the Internet of Things (IoT) [23] and consumer markets. Cost, footprint and power consumption are key market requirements for such sensors, leaving performance (as resolution and accuracy) last. An Internet search can quickly show an abundance of such sensors offered by multiple manufacturers. For example, one large online distributor [24] offers more than 1500 different generics of monolithic temperature sensors recommended for new designs!

There is scope in researching performance improvements of such sensors without sacrificing their other attributes (like low power, cost and size), thus allowing them to displace more expensive solutions in precision markets, at least for applications with temperature ranges compatible to operating temperature ranges of silicon-based integrated circuits.

1.3 Goals of this thesis

This thesis researches silicon bandgap sensors aiming to reduce their errors. Their small size and low cost due to advances in manufacturing technology of integrated circuits make them a very compelling solution in many modern applications.

Total inaccuracy of a temperature sensor consists of three error quantities: offset error, gain error, and nonlinearity. In this research, the accent is put on development of circuits with improved linearity which may be used in monolithic temperature sensors, thus reducing the required number of calibration points, and therefore lowering the total cost of use in precision applications.

New circuit architectures will be proposed. Circuit design techniques and SPICE modelling will be used to design integrated temperature sensors in standard manufacturing processes for integrated circuits.

Circuits are fabricated and then submitted to a thorough prototype evaluation procedure. By performing accurate comparison calibration in an oil bath against a laboratory grade RTD thermometer, the final goal is to prove that the inaccuracy of mass-produced silicon bandgap temperature sensors can be improved.

The aim of this research is to obtain an accuracy better than $0.1K$ in the industrial temperature range of $-40°C$ to $125°C$ after only a two-point calibration in production, without the need of additional digital correction of non-linearity.

1.4 Brief summary

In Chapter 2, this thesis will discuss first the most common practical implementations of electrical temperature sensors. Both output resistance and output voltage sensors are going to be analysed. State of the art implementations will then be described and their performances, reviewed.

A proposed new bandgap temperature sensor architecture will be described in Chapter 3, and its possible variants are going to be analysed in detail. Trade-offs between performance and variants of manufacturing process will be also discussed.

A practical implementation of the proposed sensor will be covered in Chapter 3. Design decisions, simulation results will be discussed.

Technical aspects of the evaluation setup, including constraints imposed by the targeted level of accuracy will be presented in Chapter 4. Prototype measurement procedure and collected data will be processed and summarised. It will be shown that the proposed circuit may achieve a nonlinearity of $\pm 0.4°C$ in the temperature range of $-40°C$ to $125°C$.

The development of an improved version of the proposed circuit will then be covered in Chapter 5. The new architecture will also be implemented in silicon and the prototype evaluated. It will be shown that the proposed circuit may achieve a nonlinearity of $-0.065°C/+0.035°C$ in the temperature range of $-20°C$ to $125°C$.

Further research which seeks to address the residual nonlinearity of the proposed designs will then be presented as an architecture developed to the level of advanced simulation in Chapter 6. It will be shown that this topology has the potential to achieve a nonlinearity as low as $2.22mK$ in the temperature range of $-40°C$ to $125°C$.

Also, the development of an architecture of a suitable sigma-delta analogue-to-digital converter (ADC) to process the output of the temperature sensing circuit will further be investigated. A new mathematical method of describing the operation of feed-forward discrete time second-order sigma-delta topologies will be discussed in Chapter 7, and a multi-bit ADC architecture suitable for DC signals while maintaining good linearity will be proposed in Chapter 8.

Finally, in Chapter 9, the measured performance of this work will be discussed in relation with other state of the art temperature measurement solutions. Figures of merit established in the field will be used to make meaningful comparations. Conclusions will be drawn, and it will be established in what degree the initial research goals will have been achieved along with future avenues for research uncovered during this work.

Chapter 2
Practical implementations of electrical temperature sensors

Discussed in this chapter is implementation of most common electrical temperature sensors, as well as electronic circuitry required to process their output signals. RTDs, thermistors, diodes, bandgap circuits and silicon diffusivity temperature sensing mechanisms will be analysed. State of the art integrated implementations will also be presented in detail.

2.5 Bandgap sensors

If two bipolar transistors share process parameters and operate at the same junction temperature, but at different current densities, equation (2.14) may be used to determine the difference between the base-emitter voltages of the two transistors as

$$\Delta V_{BE}(T) = V_{BE_2}(T) - V_{BE_2}(T) \cong \frac{kT}{q} \cdot \ln \frac{J_{C_2}(T)}{J_{C_1}(T)} \ , \tag{2.18}$$

where $J_{C_1}(T)$ and $J_{C_2}(T)$ are the collector current densities of the two transistors. Furthermore, if the circuit is designed in such a way that the two current densities are in a predetermined ratio n, not dependent on temperature, (2.18) may be simplified to

$$\Delta V_{BE}(T) \cong \frac{kT}{q} \cdot \ln n \, . \tag{2.19}$$

This equation states that the difference between the base-emitter voltages of two transistors biased with same-type collector currents is Proportional To Absolute Temperature (PTAT), and therefore a temperature sensor. Equation (2.19) describes accurately the temperature variation of a ΔV_{BE} voltage when the transistors operate at collector currents significantly larger than saturation currents and base width modulation is not present.

Chapter 3
A New High Performance Temperature Sensor (HPTS) Architecture

A silicon integrated temperature sensing circuit with voltage output should have low sensitivity to mismatches between its components, good power supply rejection and low output impedance [61] [62]. Low output impedance is a key factor in improving the signal to noise ratio by allowing cascading of multiple temperature sensing circuits and thus adding up their output signals.

Staring with Prof. Marinca's original patent [63], a new cell topology is proposed and further improved to generate a PTAT voltage [64].

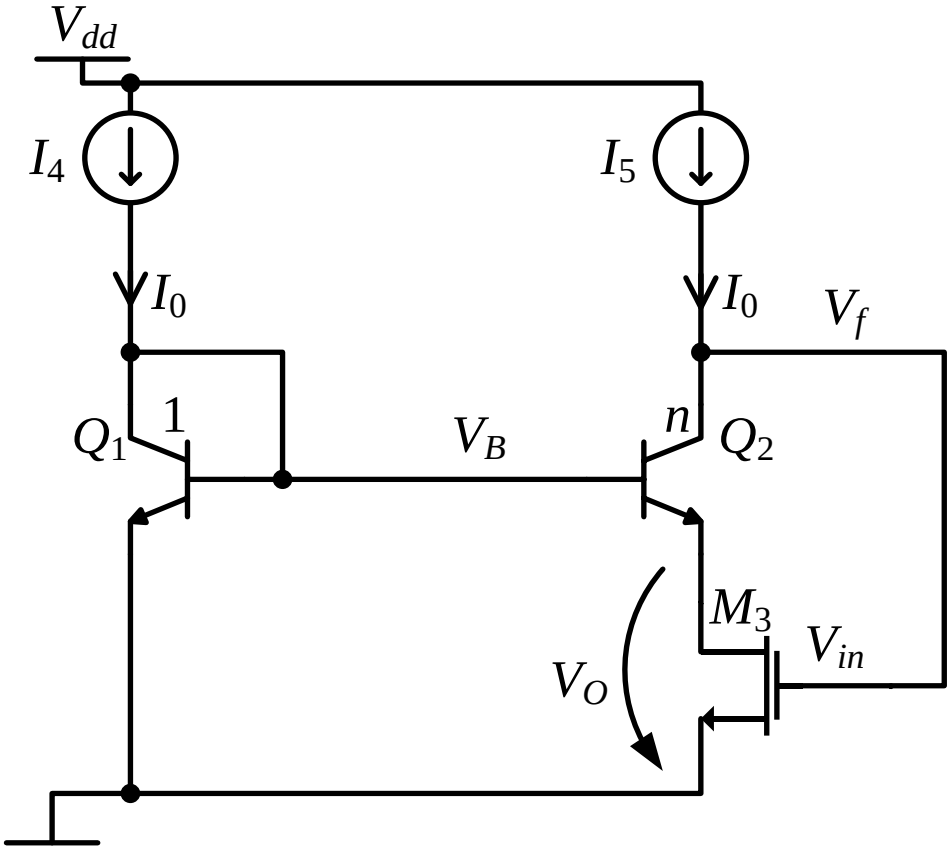


Figure 3.1. Proposed ΔV_{BE} cell. Simplified schematic.

3.1 HPTS circuit and basic operation

Studying the simplified schematic of Figure 3.1, we can see that transistor Q_1 operates at high collector current density and transistor Q_2 operates at low collector current density.

Transistors Q_2 and M_3 form a nested amplifier. The output voltage develops across the channel of transistor M_3, as shown in (2.19). We will analyse this topology from the perspective of immunity to Early effect and offset voltage of M_3. We will also assess the output resistance and variation of supply current with load.

As described by equation (2.19), the nominal output of bandgap temperature sensors does not depend on their supply current. A simple SPICE simulation highlighting this property of bandgap temperature sensors is shown in Figure 3.6.

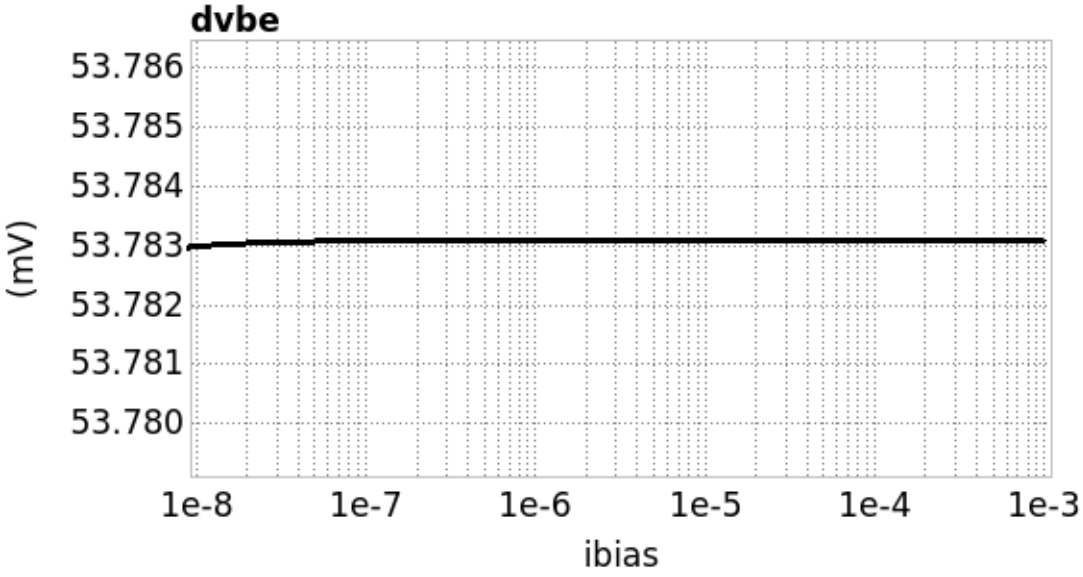


Figure 3.6. Simulation of output voltage of the proposed cell as a function of biasing current.

The simulation assumes ambient temperature of $27°C$ and a current density ratio of $n = 8$. The value of biasing current sources $I_4 = I_5 = ibias$ is swept during the simulation. Conventional bandgap temperature sensors discussed in section 2.5 rely on resistors to develop a ΔV_{BE} voltage. Therefore, they require a large die area when operating at reduced bias currents. An important advantage of the proposed cell is the ability to operate with very low bias currents (in the nA range) only by scaling currents using active current mirrors, which require significantly less area than resistor-based topologies.

Chapter 4
Silicon Implementation of HPTS and Measurement Results

Variants of the proposed architecture have been implemented in various process technologies. One implementation is discussed in detail in this chapter: a standard CMOS implementation in 0.18μm 3.3V TSMC.

4.1 CMOS implementation

The temperature sensor embedded in AD7124 [67], a low power Sigma-Delta industrial precision ADC developed and manufactured by Analog Devices, relies on a stack of ΔV_{BE} generating cells using the CMOS variant of the architecture discussed in Chapter 3. The parts are fabricated in standard 0.18μm CMOS process from TSMC.

4.1.1 CMOS circuit design

The temperature sensor in AD7124 is implemented as a stack of five cells as described in section 3.2. Its architecture and top level circuit schematic are shown in Figure 4.2 and Figure 4.3 respectively. The circuit operates of a regulated supply of $1.9V \pm 100mV$.

Matching of the current sources implemented with PMOS transistors determines the variability of the sensitivity of the temperature sensor which, for a circuit implemented with a stack of four cells and one double output cell with $1:48$ current density ratio, is approximately $2mV/°C$ nominally. Stacking of cells is also beneficial in reducing the mismatch error. If mismatch of the current sources changes with temperature, it will translate directly into non-linearity of the temperature sensor.

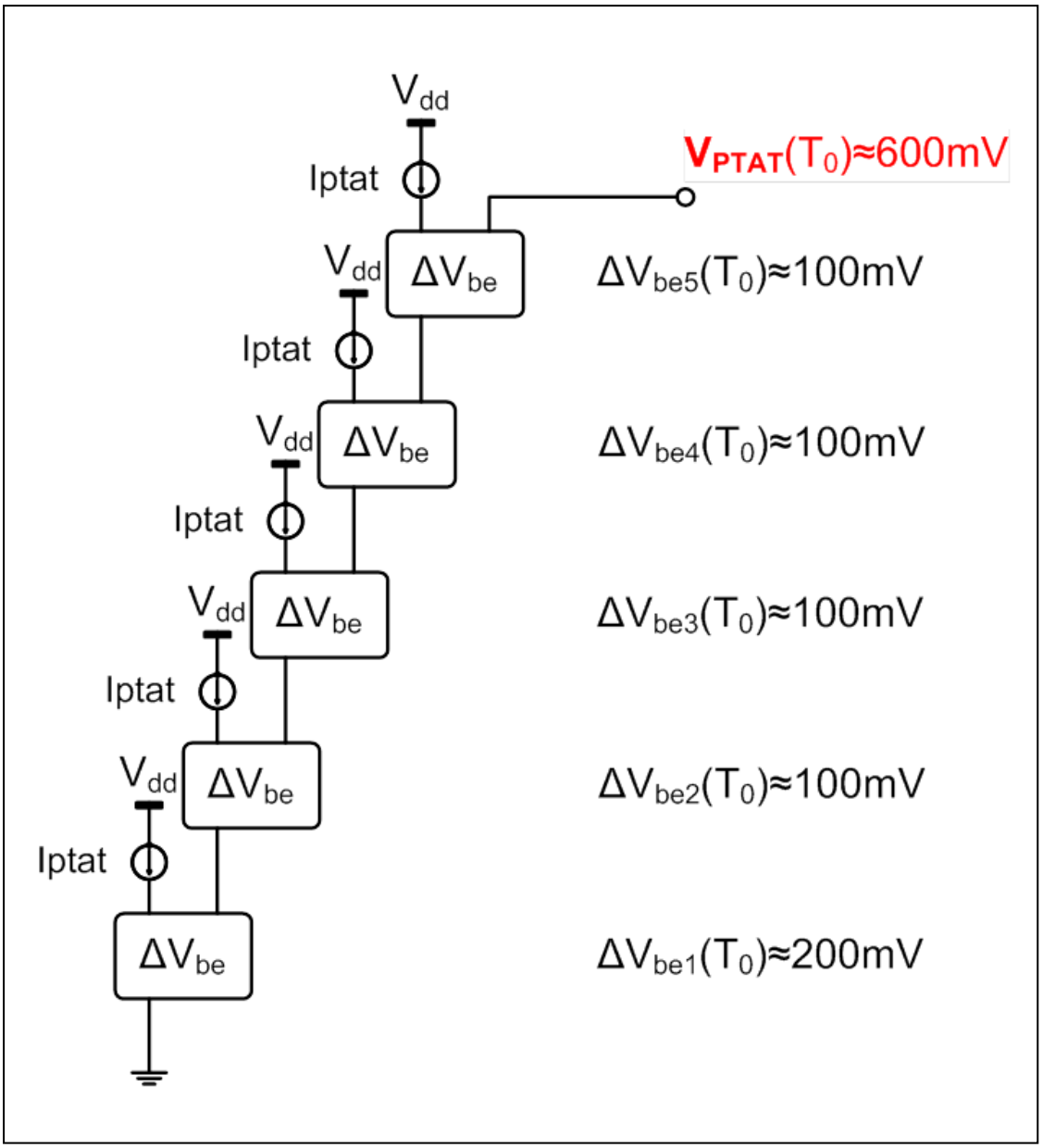


Figure 4.2. Architecture of the temperature sensor in AD7124.

4.1.2 CMOS circuit simulation results

SPICE simulations were performed on the schematic of the temperature sensor to determine circuit operation across process corners, voltage supply variation, bias current variation, and temperature.

A second set of simulations was run to determine stability of all feed-back loops. Two feed-back loops were analysed in each cell. One loop consists of the nested amplifier. The second loop provides base currents to the BJT pair.

A third set of simulations was run to determine temperature sensitivity and output variation across simulation conditions. The results are shown in Figure 4.18.

The predicted sensitivity of $2mV/°C$ is observed in simulation. A variation of $210.8\mu V$ corresponding to a temperature inaccuracy of $\pm 0.053°C$ is observed.

Finally, a 200 trials Monte-Carlo simulation was performed for nominal conditions to assess the impact of mismatch in the PMOS current sources. A mismatch-induced variation of $1.714mV$ is observed, corresponding to a temperature inaccuracy of $\pm 0.429°C$. It is obvious that mismatch is the dominant cause for temperature inaccuracy of the proposed design.

4.1.3 Silicon evaluation of the CMOS implementation

Initial evaluation of the CMOS temperature sensor using a temperature forcing system [72] showed sensor accuracy better than that of the temperature measurement system used in the lab. A more accurate method of evaluation was used subsequently.

A lot of 30 devices were evaluated in oil bath over $-40°C$ to $125°C$ and measurements shown in Figure 4.20 indicated an offset variability of $\pm 3\sigma = \pm 1.15°C$.

After removing the offset and gain errors by performing a two-point linear calibration at $25°C$ and $85°C$, the remaining nonlinearity was found very consistent and better than $\pm 0.4°C$, as in is shown in Figure 4.21.

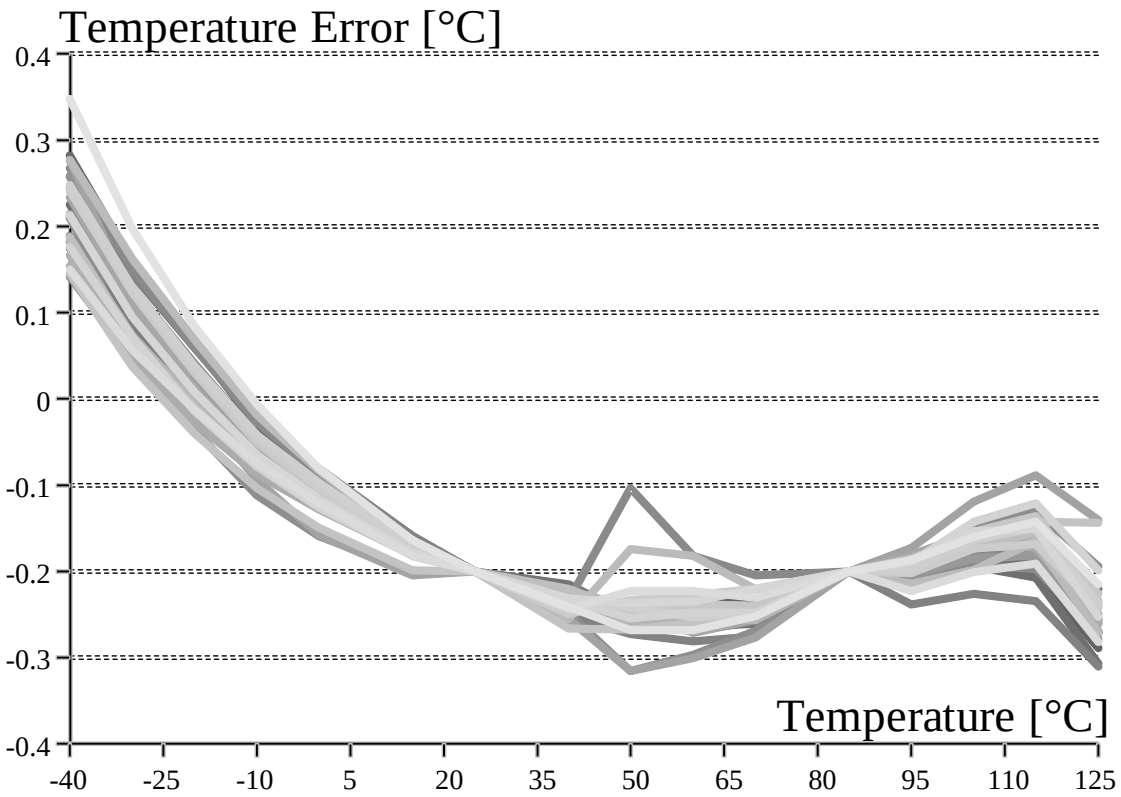


Figure 4.21. Nonlinearity of CMOS sensor after two-point calibration.

Chapter 5
An Ultra-High Performance Temperature Sensor (UHPTS)

All variants of the proposed cell discussed in Chapter 3 may be implemented in standard CMOS process technologies. However, as shown in Figure 4.18, their linear behaviour versus absolute temperature is ultimately limited by matching of the current sources used.

5.1 UHPTS complementary BJT double output cell variant

The cell reported in [73] [74] and discussed in this chapter utilizes good intrinsic matching of bipolar devices to control current density ratios and achieve increased linearity in the analogue domain. A simplified schematic is shown in Figure 5.1. The topology relies on relatively good tracking between current gain factors β of NPN and PNP transistors.

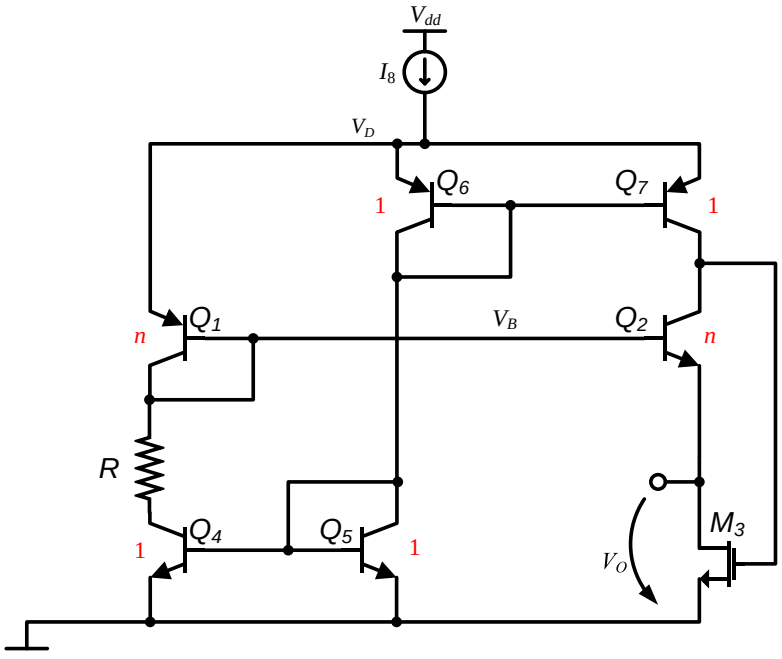


Figure 5.1. Proposed UHPTS complementary BJT ΔV_{BE} cell. Simplified schematic.

5.1.1 UHPTS complementary BJT circuit operation

Voltage V_D is established at two high current density base-emitter voltages above ground, one of the NPN transistor, Q_5 and one of the PNP transistor, Q_6. Transistors Q_1 (PNP) and Q_2 (NPN) operate at low current densities. Therefore, the output signal is a ΔV_{BE} type voltage (developed across the channel of NMOS transistor M_3) which is a proportional to absolute temperature (PTAT) signal.

The "direct" path of the nested amplifier (shown in blue) consists of transistor M_3 which operates in a common source configuration. The gain of this path is close to unity due to loading of this transistor by the low emitter impedance of Q_2.

However, the "feed-back" path provides gain in excess of 60dB through active transistors Q_2 and Q_7 which act as a push-pull (class AB) gain stage.

This configuration splits a single bias current into three equal currents using bipolar mirrors $Q_6 - Q_7$ and $Q_5 - Q_4$ with low part to part variation and reduced silicon area. The presence of a second active transistor in the feedback path boosts the total loop gain which further reduces the contribution of the offset of the nested amplifier to the output signal.

5.2 BiCMOS implementation

The improved UHPTS sensor, reported in [73], which aims to reduce part-to-part offset variations and the noise contribution of the biasing current sources is implemented as part of a test chip in 0.6μm EP134 internal process from Analog Devices, using 5 stacked cores each biased with $1.5\mu A$ PTAT current and having a high to low current density ratio $n = 16$.

Nominal temperature sensitivity is $10k/q \cdot \ln(16) \cong 2.389 mV/K$, with a nominal output voltage of $712.35mV$ at $25°C$.

5.2.2 UHPTS circuit simulation results

Each core draws $1.55\mu A$ IDD current and the bias current generator uses an additional 2.2μA. The power consumption of the temperature sensor at 3.0V supply is $29.85\mu W$.

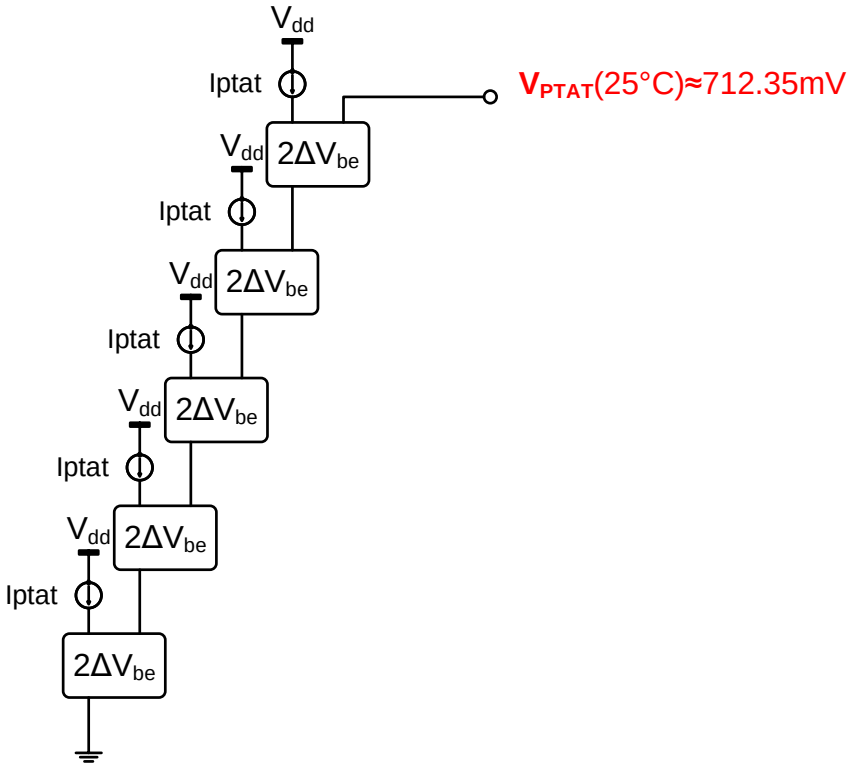


Figure 5.4. Architecture of the temperature sensor on BiCMOS test chip.

SPICE simulations of the proposed design were run to determine the nonlinearity of the temperature sensing cells. Figure 5.10 shows a single temperature sweep simulation under nominal conditions. A second simulation was run across five process corners for the stack of five temperature sensing cells. The results are shown in Figure 5.11. Simulated nonlinearity across the $-40°C$ to $125°C$ temperature range is less than $\pm 3.5\mu V$, corresponding to a temperature inaccuracy of $\pm 1.5mK$.

5.2.3 Silicon evaluation of the BiCMOS implementation

The die was packaged in a standard 32 pin LFCSP plastic package. An oil bath setup was used to evaluate a lot of 23 devices randomly chosen from the same wafer.

Nonlinearity of the fabricated parts was measured against a Hart 1590 Super-Thermometer with an accuracy specification of $1ppm$.

The measured average temperature sensitivity was $2.465mV/K$, with a spread of $\pm 2.01\mu V/K$.

Measured temperature inaccuracy is shown in Figure 5.15. After removing a systematic offset of $-13.7mV$ and using the average sensitivity value, the batch calibrated spread at $25°C$ was found to be better than $\pm 0.5°C(3\sigma)$.

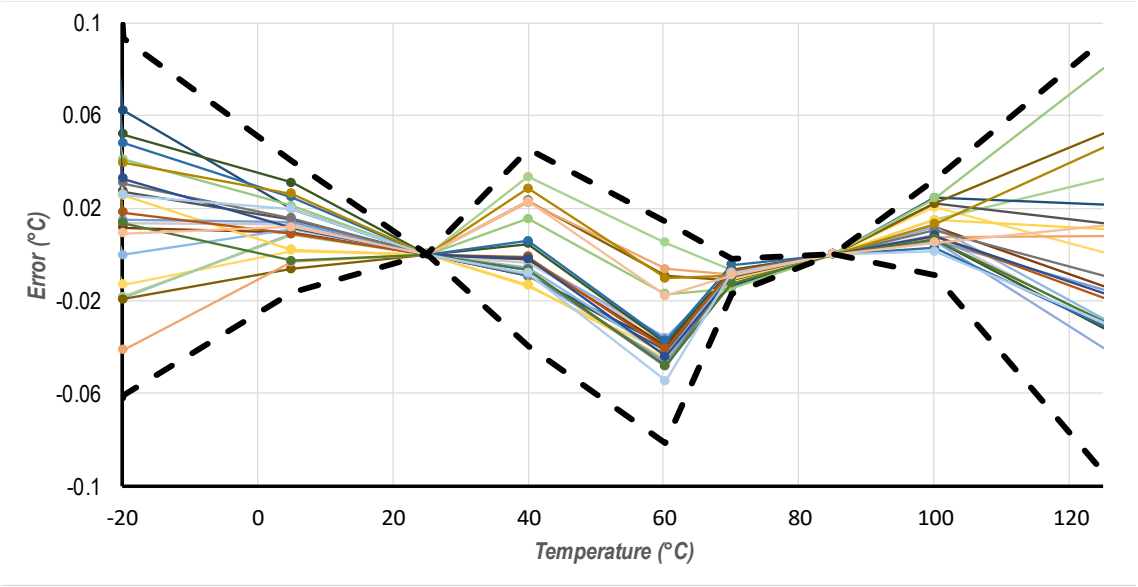


Figure 5.15. Measured temperature inaccuracy of the proposed BiCMOS sensor; 3σ limits shown with dotted lines.

After two-point calibration at $-10°C$ and $80°C$, total inaccuracy drops to $-0.065°C/+0.035°C$ (3σ), as can be seen in Figure 5.15.

Noise was measured for 5 parts in oil bath at $25°C$ in $0.1Hz$ to $50Hz$ bandwidth. The measured value of $0.287\mu V$ RMS corresponds to a temperature resolution of $0.12mK$ RMS.

5.2.4 Figure of merit of the BiCMOS implementation

To evaluate the proposed temperature sensor architecture against previously reported circuit architectures, two Figure of Merit (FoM) calculations proposed by Kamran Souri and Kofi Makinwa [75] have been used.

Resolution FoM for temperature sensors is defined as the product of energy/conversion and the square of resolution, which is limited by the signal to wide band noise ratio. For the proposed design, it is evaluated at $4.3\,fJ\cdot K^2$.

Inaccuracy FoM is measured as the product of energy/conversion and the square of relative inaccuracy, as different temperature sensors might be specified across different temperature ranges. For the proposed design, it is evaluated at $1.11nJ\cdot\%^2$.

Chapter 6
Mitigation of residual nonlinearity in bandgap temperature sensors

Nonlinearity and ultimately total inaccuracy of the improved precision temperature sensor discussed in Chapter 5 is limited by Early effects of the bipolar transistors implementing the temperature sensing cell. Discussed in this chapter are the theoretical background of nonlinearity errors induced by direct and ***reverse*** Early effects, as well as a circuit topology which may address these errors.

6.2 An advanced circuit topology which mitigates reverse Early effects

A simplified schematic of the new topology [79] is shown in Figure 6.1.

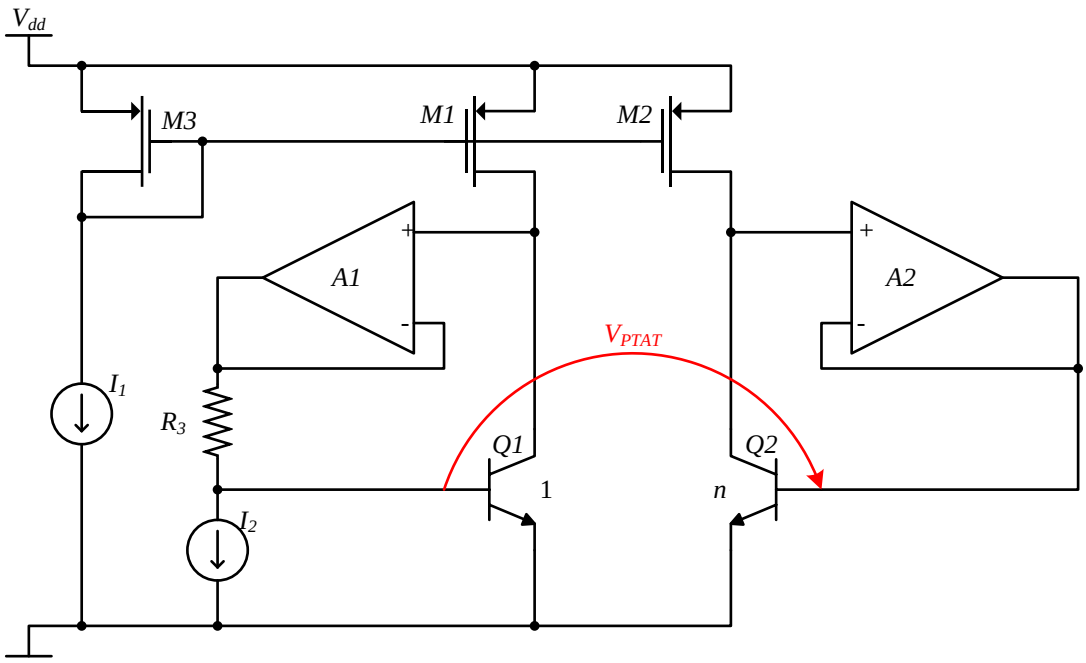


Figure 6.1. PTAT voltage circuit with Early voltage compensation as reported in [79].

To compensate for Early voltage effects, the two transistors generating the base-emitter voltage difference are biased differently: transistor Q_2 (operating with low collector current density) operates in virtual diode mode, with zero base-collector voltage and base current provided by amplifier A_2; transistor Q_1 (operating with high collector current density) has its collector-base voltage equal to the voltage drop across resistor R_3.

6.3 Simulation of ultra-linear temperature sensing circuit

A circuit according to Figure 6.1 was simulated in a low geometry BiCMOS process. I_1 was implemented as a $3\mu A$ PTAT current generator at ambient temperature ($T_0 = 300K$). The aspect ratio of M_1, M_2 and M_3 is 1:1:1. The high collector current density transistor Q_1 is implemented as a unit vertical NPN device; the low collector current density transistor Q_2 is implemented as eight unit BJTs connected in parallel. Therefore, the ratio of current densities is $n = 8$. Vertical NPN transistors in this process have the forward Early voltage $V_{AF} = 52.2V$ and the reverse Early voltage $V_{AR} = 5.89V$. The ideal value of the generated base-emitter voltage difference at ambient temperature T_0 is $\Delta V'_{be0} \cong 53.76mV$.

Therefore transistor Q_1 must be biased with a collector-base voltage

$$V_{CB_0}^{(Q_1)} \cong \Delta V'_{BE} \cdot \frac{V_{AF}}{V_{AR}} \cong 478mV \tag{6.6}$$

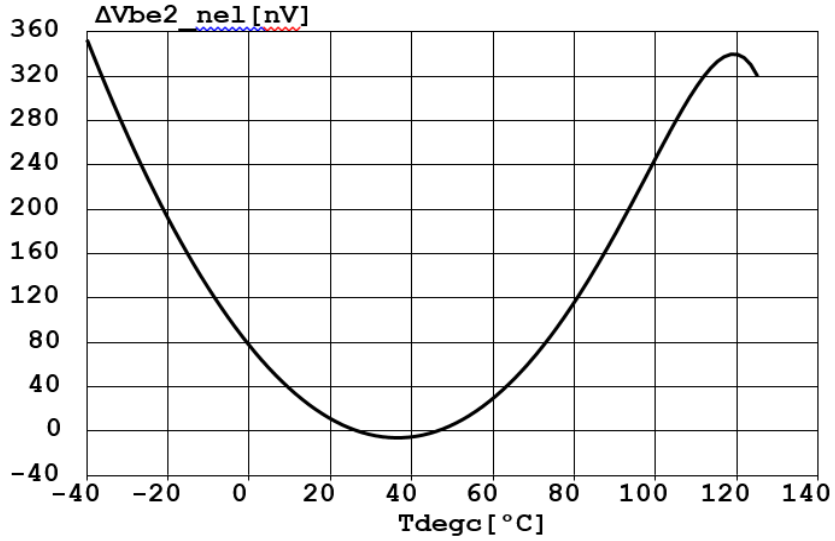


Figure 6.5. Nonlinearity of the PTAT voltage of Figure 6.2, for $V_{CB_0}^{(Q_1)} = 577mV$ *and* $V_{CB}^{(Q_2)} = 0$.

The sensitivity of the PTAT voltage is $0.18 mV/K$.

An advanced compensation can be achieved if the collector-base voltage of Q_1 is set to an optimum value to compensate the higher order parameters not taken into account in the hand calculation. A new collector-base voltage of $577mV$ was set and the circuit of Figure 6.1 resimulated. The new nonlinearity is presented in Figure 6.5. Note the Y-axis scale: it is 500 times smaller than the Y-axis scale in Figure 6.3. This nonlinearity of less than $400nV$ corresponds to $2.22mK$. The improvement factor in linearity of the $PTAT$ voltage with Early voltages compensation vs. prior art implementation is greater than 450.

6.4 Rationale for using an ADC with the ultra-linear temperature sensing circuit

As seen in Figure 6.1, the ultra-linear temperature sensing circuit discussed in this chapter has a floating output, the differential voltage between the base potentials of transistors Q_1 and Q_2. Also, the output resistance of the circuit at the base of transistor Q_1 is dominated by the value of resistor R_3. Therefore, an ADC would be suitable for extracting the highly linear temperature-dependent signal from the proposed circuit, as shown in Figure 6.6.

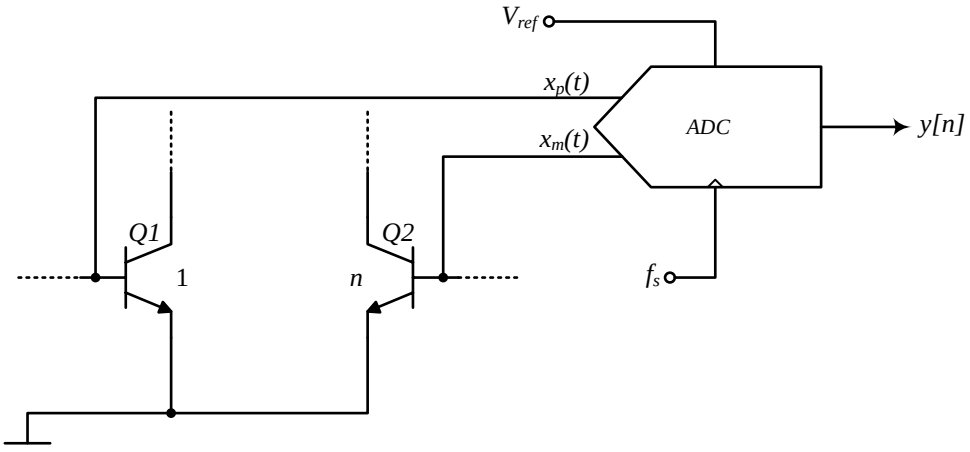
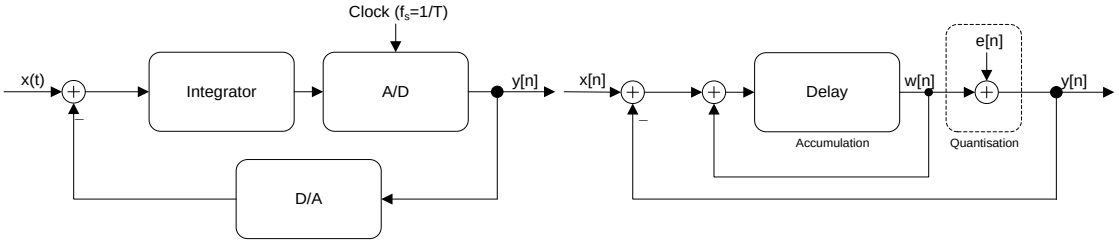


Figure 6.6. Using a differential ADC to process the output of the ultra-linear temperature sensing circuit.

The analogue differential signal $x(t) = x_p(t) - x_m(t)$ is sampled at frequency f_s and converted into a data stream $y[n]$ using the reference voltage V_{ref}. A high linearity ADC architecture capable of converting low bandwidth, down to DC, differential signals with arbitrary common mode is required. Therefore, a discrete time (DT) sigma-delta (ΣΔ) ADC architecture will be investigated in the following chapters.

Chapter 7
A high linearity Sigma-Delta ADC architecture

As most monolithic temperature sensors with digital output contain a sigma-delta ADC [39] [41] [58] [60], presented in this chapter is an original attempt at providing a general form of the transfer functions which describe the operation of a feed-forward analogue-to-digital [81] ΣΔ modulator. The general equations are validated by being applied to a single-bit switched capacitor implementation.



(a)(b)

Figure 7.1 (a) Block diagram of a ΣΔ modulator; (b) Sampled-data equivalent circuit

We assume that the modulator contains a multilevel, uniform quantiser with unity gain $G=1$. The input to the circuit feeds to the quantiser via an integrator, and the quantised output feeds back to subtract from the input signal, as shown in Figure 7.1(a).

7.4 MASH 2−2 modulator

Figure 7.16 shows a generalised cascade of two ΣΔ modulators. This structure is also called multi-stage or MASH (for Multi-stAge noise SHaping) [83]. The second modulator converts the error from the first modulator which is then digitally cancelled. This approach is equivalent to a two-step converter, where both stages are ΣΔ modulators.

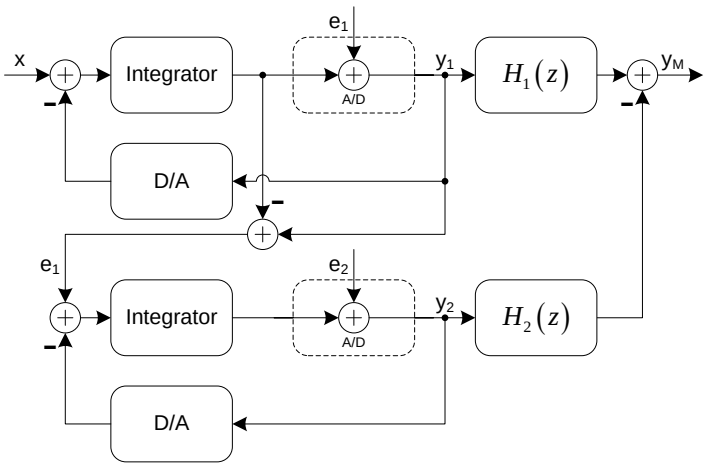


Figure 7.16. General block diagram of a ΣΔ MASH structure.

The quantisation error e_1 of the first stage is found in analogue form by subtracting the input to its quantiser from the output. This signal is used as input to a second ΣΔ loop. The output of the second loop is given by

$$Y_2(z) = STF_2(z)E_1(z) + NTF_2(z)E_2(z) \tag{7.50}$$

The digital filters $H_1(z)$ and $H_2(z)$ which process the outputs of the two ΣΔ loops are designed to achieve cancellation of the first stage error $E_1(z)$ in the output $Y_M(z)$. The cancellation is obtained if

$$H_1(z)\cdot NTF_1(z) - H_2(z)\cdot STF_2(z) = 0\,. \tag{7.51}$$

An implementation is presented in Figure 7.19.

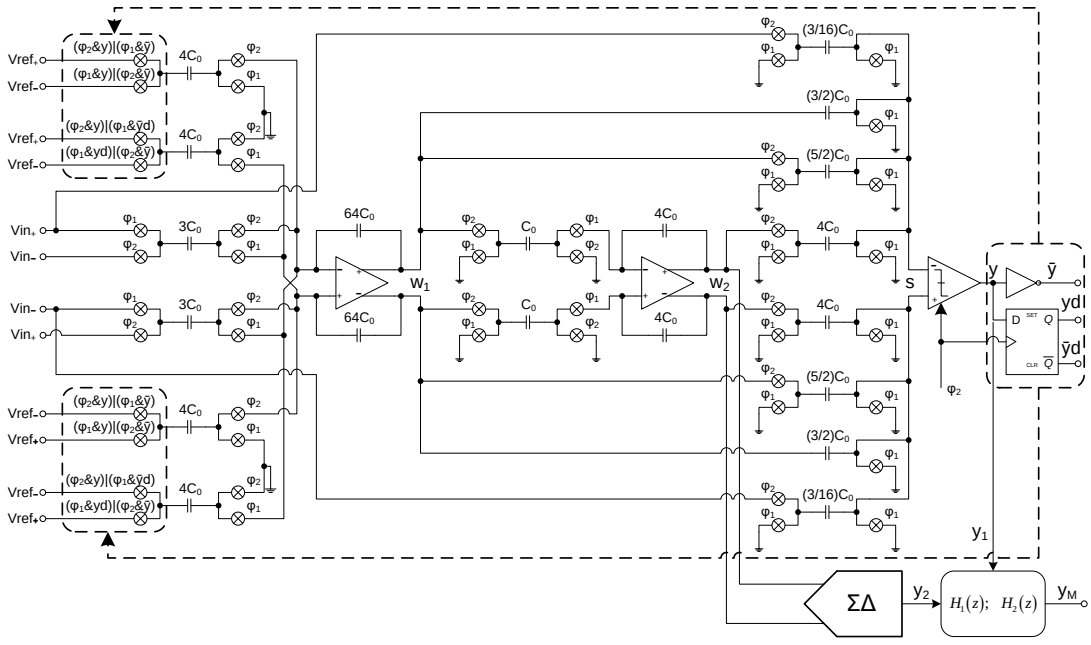


Figure 7.19. MASH 2−2 single bit feed-forward ΣΔ modulator.

Chapter 8 A Discrete-Time Sigma-Delta ADC with Multi-bit Feed-back Loop

As our temperature sensing circuit architectures may operate with a wide range of biasing currents, and therefore very low power circuits may be constructed, we will investigate how total power required by a DT ΣΔ ADC may be reduced by increasing the number of bits in the quantiser while maintaining linearity.

8.2 Ideal DAC performance and effects of component mismatch

The special characteristic of DACs used in the feed-back path of Sigma-Delta modulators is that their accuracy requirements are dictated by the precision of the ADC, unlike the case of standard DACs which must be accurate to only $\pm 1/2$ of their LSB. Simulations were performed using a full-scale sine-wave input signal such that the oversampling rate would be $OSR = F_s/2f_{in} = 512$. The effect of unit elements mismatch can be observed in Figure 8.5.

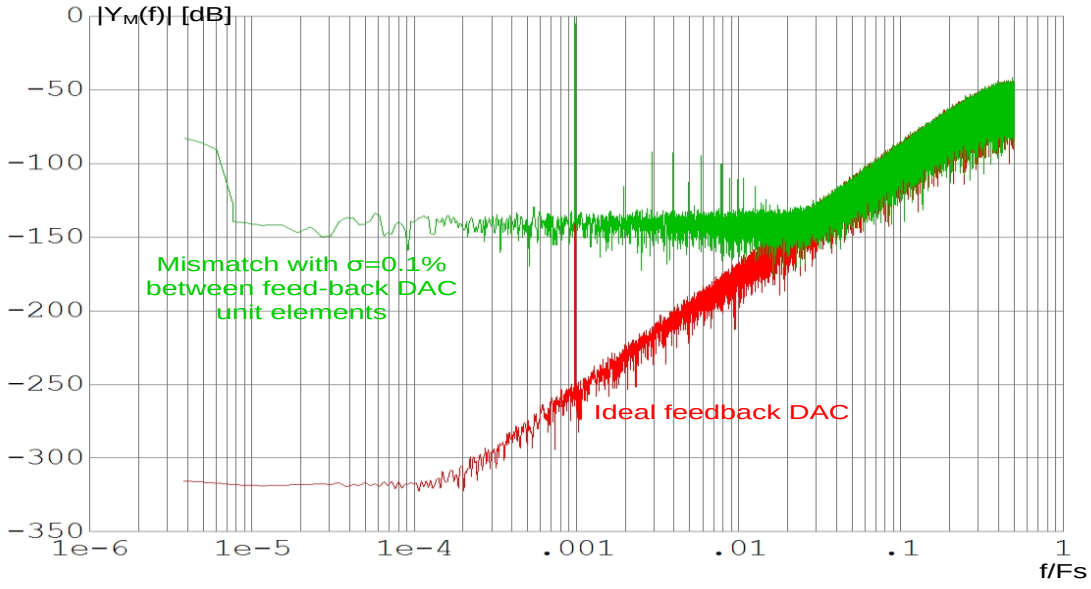


Figure 8.5. Effects of unit elements mismatch in the feed-back DAC.

8.3 Noise-shaped element usage

It is possible to apply the noise-shaping principle to the errors caused by element mismatch [84] [85]. By modulating the element control signals using ΣΔ techniques, the element mismatch errors will have a noise-shaped spectrum. Every element will have similar usage history *on average*.

8.4 Power analysis

Having established in the previous section that a solution for a multi-bit DAC can be used in a system with good DC performance, and that signal swings in such a converter can be predicted accurately, this section focuses on estimating the power savings which can be achieved when replacing a single-bit architecture with a multi-bit implementation. This estimation does not account for the excess current required in the digital side of the converter.

8.4.1 Estimation of the supply current required by the integrators

The switched capacitors integrator presented in Figure 7.10 is presented in simplified form in Figure 8.9. We assume that the switches are made with on resistance low enough not to affect settling in a substantial way. Power requirements are estimated based on supply current needed for settling in the integrators.

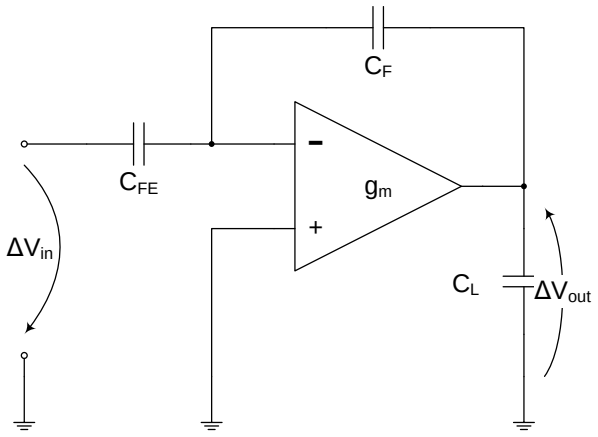


Figure 8.9. Simplified schematic of a switched capacitors integrator used to analyse settling.

Based on B, the number of bits in the feedback path,

$$\left|\Delta V_{out}\right|_{\max} = \frac{2}{2^B - 1} \cdot \frac{V_{ref} C_{ref}}{C_F} \quad . \tag{8.44}$$

Assuming that $V_{in_{\max}} = V_{ref}$ and using equation (8.30),

$$C_{in} \le \left(1 - \frac{2}{2^B - 1}\right) C_{ref} \text{ for } B > 2 \, . \tag{8.45}$$

For $B \le 2$, C_{in} must be chosen smaller than C_{ref} (for linearity reasons), typically $C_{in} / C_{ref} = K = 0.75$. This does not affect the result in (8.44) for $B = 2$ and for single bit where zero code at the input of the internal DAC is allowed.

8.4.4 Total settling time

Total settling time can be estimated as

$$\begin{aligned} t_{settle} &= t_{slew} + t_{ss} \\ &= \frac{2}{2^B - 1} \cdot \frac{C_{ref} V_{ref}}{R I_{dd}} + 22 \cdot \frac{kT}{q} \cdot \frac{\left(3 - \frac{2}{2^B - 1}\right) C_{ref}}{n R I_{dd}} \, , \\ &= \frac{C_{ref}}{R I_{dd}} \cdot \left(V_{ref} \cdot \frac{2}{2^B - 1} + \frac{22}{n} \cdot \frac{kT}{q} \cdot \left(3 - \frac{2}{2^B - 1}\right)\right) \end{aligned} \tag{8.54}$$

or, for single-bit feedback,

$$\begin{aligned} t_{settle} &= t_{slew} + t_{ss} \\ &= (1 + K) \cdot \frac{C_{ref} V_{ref}}{R I_{dd}} + 22 \cdot \frac{kT}{q} \cdot \frac{(2 + K) C_{ref}}{n R I_{dd}} \\ &= (1 + K) \cdot \frac{C_{ref}}{R I_{dd}} \cdot \left(V_{ref} + \frac{22}{n} \cdot \frac{kT}{q} \cdot \frac{(2 + K)}{(1 + K)} \right) \end{aligned} \tag{8.55}$$

8.5 Estimated figure of merit improvement

As all other parameters of the converter are kept similar, the improvement in figure of merit for a multi-bit implementation is about $17.5 dB$.

Chapter 9
Conclusions

A review of the concept of temperature and methods used to measure it has been conducted in this work. Based on the current state of the embedded temperature sensing landscape, a need for low cost, yet precise temperature measurement devices was identified. New circuit topologies were invented, and circuits were constructed and evaluated which showed significant performance improvements compared to existing prior art in the field. Also, a multi-bit discrete time sigma-delta analogue to digital converter architecture suitable for DC signals (like those output by bandgap temperature sensors) was developed.

9.1 Original contributions and discussion of results

All material presented in Chapter 3, Chapter 4, Chapter 5, Chapter 6, Chapter 7, and Chapter 8 (except the circuit shown in Figure 3.14, which was proposed by Art Kalb and John Shafran) represents original work of the author, under guidance from prof. dr. Stefan Marinca and prof. dr. Mircea Bodea. This includes development of the architecture of each cell variant, of the sigma-delta ADC, circuit design and implementation, as well as interpretation of measured silicon results.

Also, the MEMS structure shown in Figure 2.3 is based on original work of the author, not published previously.

The original contributions presented in this thesis are summarised as follows:

(1) A new circuit architecture was developed for a high precision temperature sensor [64]. An embodiment of the architecture was designed, fabricated, evaluated and released as part of a commercially available product of Analog Devices Inc. (AD7124) [67]. A non-linearity of $\pm 0.4°C$ across temperature range of $-40°C$ to $125°C$ may be achieved after an only two-point calibration. This performance compares favourably against commercially available monolithic temperature sensors [24].

(2) An improved complementary BJT circuit architecture for an ultra-high precision temperature sensor was developed subsequently [73]. The architecture was implemented as a design in a BiCMOS technology process, fabricated and evaluated as a prototype. A non-linearity of $-0.065°C/+0.035°C$ was achieved across temperature range of $-20°C$ to $125°C$ after performing a two-point calibration.

As it can be observed in Table 9.1, the proposed temperature sensor design offers the lowest noise, inaccuracy and voltage supply sensitivity while maintaining comparable area and power consumption in relation to other state of the art designs.
Intrinsic linearity allows the proposed architecture to obtain a resolution figure of merit significantly better than other state of the art designs.
The figures of merit established in literature were modified for purely analogue temperature sensors.

Table 9.1. Performance summary and comparison to previous work.

	This work	ISSCC12 [59]	CICC13 [92]	ISSCC14 [58]	ISSC16 [41]
Technology	0.6µm BiCMOS	0.16µm CMOS	0.18 µm CMOS	0.7µm CMOS	40nm CMOS
Type	BJT	BJT	CMOS	BJT	TD
Area	$0.31mm^{2}$ [a1]	$0.08\ mm^{2}$	$0.09mm^{2}$	$0.8mm^{2}$ [a2]	mm^{2}
Supply Voltage	3.0V-5.5V	1.5V-2.0V	1.2V	2.9V-5.5V	0.9V-1.2V
Temperature Range	-40°C to 125°C	-55°C to 125°C	0°C to 100°C	-45°C to 130°C	-40°C to 125°C
Calibration	2 points	1 point	2 points	1 point	1 point
Inaccuracy	+0.035°C / −0.065°C[c]	±0.15°C[b]	+1.3°C / −1.4°C[c]	±0.15°C[b]	±0.75°C[b]
Power	29.85µW[a]	6.12µW	65nW	181.5µW[d]	2.5mW
Supply sensitivity	0.033°C/V	0.5°C/V	–	0.05°C/V	–
Resolution (meas. time)	0.16mK (10ms)	20mK (5.3ms)	0.3K (31.25ms)	30mK (2.2ms)	0.36K (1ms)
Resolution FoM	$4.3fJ{\cdot}K^{2}$	$11pJ{\cdot}K^{2}$	$0.18nJ{\cdot}K^{2}$	$0.36nJ{\cdot}K^{2}$	$32.4\mu J{\cdot}K^{2}$
Accuracy FoM	$1.11nJ{\cdot}\%^{2}$	$0.75nJ{\cdot}\%^{2}$	$14.8nJ{\cdot}\%^{2}$	$11.7nJ{\cdot}\%^{2}$	$2.05\mu J{\cdot}\%^{2}$

(3) The proposed architecture also achieves a very good accuracy figure of merit without the need for digital correction. Thus, it enables multiplexing of multiple accurate temperature sensing channels with ease using standard analogue to digital converters.

While thermal diffusivity sensors can operate at lower supply voltages [41] and CMOS-based temperature sensors can be scaled down to very low power levels [92], BJT-based sensors remain competitive in applications which require very good accuracy at limited power.

(4)A new ultra-linear circuit was developed to the stage of advanced SPICE simulation [79]. This circuit addresses the non-linearity induced by Early effects and pushes the achievable non-linearity down to $2.22mK$ across temperature range of $-40°C$ to $125°C$. Therefore, a solution to the fundamental problem of compensation of reverse Early effects, present in bandgap temperature sensors is proposed.

(5) Original general equations describing signal and noise transfer functions of feed-forward discrete time sigma-delta modulators were derived and validated using switched-capacitors circuit blocks.

(6) These equations were used to construct a MASH2-2 multi-bit discrete time sigma-delta ADC suitable for floating differential DC input signals, with significant figure of merit improvements vs. single-bit designs.

9.2List of original works

1. John O'Dowd, Andreas Callanan, Gabriel Banarie, Enrique Company-Bosch – Capacitive sensor interfacing using sigma-delta techniques – SENSORS, 2005 IEEE.
2. John O'Dowd, Damien McCartney, Gabriel Banarie – One terminal capacitor interface circuit – US7235983B2, grant date 26/06/2006.
3. John O'Dowd, Damien McCartney, Gabriel Banarie – One terminal capacitor interface circuit – US7304483B2, grant date 04/12/2007.
4. Gabriel Banarie, Andreas Callanan, Damien McCartney, Colin Lyden – Techniques for calibrating measurement systems – US9389275B2, grant date 12/07/2016.
5. Gabriel Banarie, Adrian Sherry – Stability correction for a shuffler of a Σ-delta ADC – US8653996B2, grant date 18/02/2014.
6. Adrian Sherry, Gabriel Banarie, Roberto Maurino – Method and apparatus for separating the reference current from the input signal in sigma-delta converter – US9124290B2, grant date 01/09/2015.
7. Stefan Marinca, Gabriel Banarie – A novel high precision temperature sensor – 26th Irish Signals and Systems Conference (ISSC) 2015 IEEE.
8. Stefan Marinca, Gabriel Banarie – Voltage reference circuit – US9600014B2, grant date 21/03/2017.
9. Viorel Bucur, Gabriel Banarie, Stefan Marinca, Mircea Bodea – An embedded charge pump for a Zener-based voltage reference compensated using a ΔVBE stack – 24th International Conference "Mixed Design of Integrated Circuits and Sistems", MIXDES 2017 IEEE.
10. Paraic Brannick, Colin Lyden, Damien McCartney, Gabriel Banarie – Analog/digital converter with charge rebalanced integrator – US9806552B2, grant date 31/10/2017.

11. Stefan Marinca, Gabriel Banarie, Viorel Bucur, Mircea Bodea – A ±2m°C linearity silicon temperature sensor – International Symmposium on Signals, Circuits and Systems (ISSCS) 2017 IEEE.
12. Roberto Maurino, Sanjay Rajasekhar, Pasquale Delizia, Colin Lyden, Gabriel Banarie – Precision low noise continuous time sigma delta converter – US9800262B1, grant date 24/10/2017.
13. Viorel Bucur, Gabriel Banarie, Stefan Marinca, Mircea Bodea – A Zener-Based Voltage Reference Design Compensated Using a ΔVBE Stack – 25th International Conference "Mixed Design of Integrated Circuits and Systems" (MIXDES) 2018 IEEE.
14. Gabriel Banarie, Declan McDonagh, Viorel Bucur, Stefan Marinca, Mircea Bodea – A BJT BiCMOS Temperature Sensor with a Two-Point Calibrated Inaccuracy of 0.1°C (3σ) from -40 to 125°C – 29th Irish Signals and Systems Conference (ISSC) 2018 IEEE.
15. Andreas Callanan, Adrian Sherry, Gabriel Banarie, Colin Lyden – Time interleaved filtering in analog-to-digital converters – US10236905B1, grant date 19/03/2019.
16. Viorel Bucur, Gabriel Banarie, Stefan Marinca, Mircea Bodea – Reducing the Bipolar Junction Transistor Vbe Non-Linearity – 26th International Conference "Mixed Design of Integrated Circuits and Systems" (MIXDES) 2019 IEEE.

9.3 Future research

The proposed UHPTS architecture was proven in silicon. Based on measurement data gathered from the BiCMOS test chip, a commercial temperature sensor product is currently developed by Analog Devices Inc.

Future avenues for research include a silicon implementation of the ultra-linear temperature sensing circuit proposed in Chapter 6 and the construction of a digital output monolithic temperature sensing circuit.

Last, but not least, temperature drifts of offset or gain coefficient of electronic circuits in plastic packages is affected by mechanical stress induced by ambient humidity or thermal expansion. Therefore, improved resilience to mechanical stress could be investigated.

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